10.3 A Silicon 60GHz Receiver and Transmitter Chipset for Broadband Communications

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A chipset for gigabit per second wireless communications in the 60GHz ISM band is presented. The two chips (RX and TX) are implemented in a 0.13µm SiGe BiCMOS technology with f_T=200GHz and f_{max}=250GHz. Envisioned applications of the chipset include 1 to 2Gb/s directional links using ASK or PSK modulation and 500Mb/s to 1Gb/s omni-directional links using OFDM modulation.

Figure 10.3.1 shows a block diagram of the RX and TX chips. A superheterodyne architecture with a variable IF is used that requires only a single PLL. Image rejection as well as IF filtering are handled on chip. Local oscillator signals for the mm-wave or IF mixers are generated by either tripling or halving the frequency of the VCO, respectively. For 59 to 64GHz operation, this architecture results in an IF of 8.4 to 9.1GHz, a VCO frequency of 16.8 to 18.3GHz, and an image frequency of 42 to 46GHz.

Figure 10.3.2 shows a schematic of the four-stage LNA used in the RX chip. Image rejection is provided in the final two stages by notch filters at 47 and 41GHz. Each notch contains a small capacitor in parallel with an open-circuited microstrip stub, λ/4 in length at the notch frequency. This creates a series resonance at the image and a parallel resonance at RF. The NF of each cascode amplifier is ~6dB; hence, stages one and two are added, each with 5 to 6dB gain and ~4dB NF. Independent LNA measurements across 59 to 64GHz show 5 to 6.2dB NF, 20dB gain, <-12dB S_{11} and S_{22}, and <-40dB S_{12}. Image rejection is >26dB; input P_{1dB} is -29dBm; and current draw is 10mA from a 2.7V supply.

The first mixer in the RX chip is single-balanced with a common-base input, similar to one described in [1], providing about 9dB of conversion gain. The RX mixer is followed by an IF VGA with 0 to 10dB of gain, quadrature IF mixers with unity gain, and unity gain baseband output buffers to drive external 100Ω differential loads. IF filtering, centered at 8.8GHz, is provided by the loads of the RX mixer and IF VGA, with a cascaded IF bandwidth > ±700MHz. The cascaded NF of the mixer and subsequent stages is 13dB at 25°C.

An integer-N PLL is included with the RX and TX. The PLL operates off of a 520 to 610MHz reference clock, generating a 16.6 to 19.5GHz output signal. The differentially-tuned VCO uses a cross-coupled bipolar topology with MOS varactors and slab inductors in the tank. Emitter-coupled logic is used for the asynchronous divide-by-32, while CMOS is used for the phase-frequency detector and charge pump. PLL measurements show a phase noise of -95 to -100dBc/Hz at 1MHz offset with an rms jitter <1.5° integrated over 1MHz to 1GHz. The PLL consumes ~75mW from a 2.7V supply and 4mW from a 1.5V supply.

The local oscillator for the RX mixer is provided by a harmonic frequency tripler [2]. The PLL output is applied to a cascoded differential pair, producing third harmonic, that goes through two stages of amplification and filtering. The differential tripler output is >560mV$_{pp}$ at the mixer switches with phase noise floor of <-132dBc/Hz.

On-wafer measurements are made on the full RX with PLL. As shown in Fig. 10.3.3, at 25°C, the RX power conversion gain is 38 to 40dB and the NF is 5 to 6.7dB. Image rejection is 30 to 40dB and input P_{1dB} is -36dBm. Note that the large LNA gain is used to trade-off linearity for NF in the RX, an acceptable trade-off in light of the 60GHz channel characteristics. The RX draws 195mA from a 2.7V supply, 50mA of which is in the baseband output buffer. At 85°C, NF remains below 8dB while gain drops by 5 to 6dB. Additional receiver measurements are summarized in Fig. 10.3.4.

The TX PA is made of two single-stage cascode amplifiers operating in a push-pull configuration from a 4V supply [3]. The linear, class-AB amplifier has 15dB gain at 61.5GHz. Measurements show a 10.5dBm output P_{1dB} and >17 dBm P_{sat}. The PAE across the ISM band is between 6 and 10%, an improvement over that achieved in [2] due to the improved PA topology.

A pre-driver amplifier is included to provide signal amplification and >25dB image rejection. A two-stage design is used—fully differential in stage one with a 47GHz notch, and balanced in stage two with a 41GHz notch. The input impedance for the pre-driver is designed to provide low impedance at the image and high impedance at RF. Measurements on the pre-driver show 8 to 12dB of gain and 6 to 8dBm output P_{1dB}. The circuit consumes 36mA from a 2.7V supply.

The IF strip in the TX is the reverse of that of the RX. Baseband I/Q signals are applied to a pair of double-balanced mixers dotted into a common RLC load. The IF VGA drives a double-balanced IF-to-RF mixer which provides a maximum signal level of -3dBm at 59 to 64GHz to the pre-driver. IF filtering is again provided by the IF mixer and IF VGA loads, with ±700MHz BW.

On-wafer measurements, summarized in Fig. 10.3.4, are made on the full TX with PLL. Figure 10.3.5 shows the measured output power and conversion gain versus I/Q input power of a 100MHz CW tone for 59, 61.5, and 64GHz. P_{1dB} is 10 to 12dBm; P_{sat} is 16 to 17dBm; and the conversion gain is 34 to 37dB. Across 5 to 85°C, P_{1dB} remains constant while gain drops by 7dB. The measured spurious response is shown in Fig. 10.3.6. At -25dBm input power, 20 to 30dB of image suppression and 20 to 25dB of carrier suppression are observed. The spur from 3×LO feedthrough is <-20dBm. No dc-offset correction is applied and the external I/Q quadrature accuracy is within ±1°. At P_{1dB}, the TX draws 190mA from a 2.7V supply and 72mA from a 4V supply.

The RX and TX ICs are packaged together with 7dBi folded-dipole antennas. BER testing of these modules has been completed using an IEEE 802.11a-based OFDM-QPSK modulation at 630Mb/s. The modulation is implemented using a 700Ms/s ARB for baseband I/Q modulation and a 700Ms/s 8b PCI ADC and software demodulator. At 630Mb/s, the setup operates error free for a 10m separation. Die micrographs of the RX and TX are shown in Fig. 10.3.7. The die sizes are 3.4×1.7mm^2 and 4.0×1.6mm^2, respectively. In conclusion, this highly-integrated 60GHz chipset is flexible enough to work in a variety of wireless systems, having already achieved a data rate of 630Mb/s over 10m.

Acknowledgments:
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References:
[1] S. Reynolds, "A 60-GHz Superheterodyne Downconversion Mixer in SiGe Bipolar Technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2065-2068, Nov., 2004.
[2] B. Floyd, *et al*., "SiGe Bipolar Transceiver Circuits Operating at 60GHz," *IEEE J. Solid-State Circuits,* vol. 40, no. 1, pp. 156-167, Jan., 2005.
[3] U. Pfeiffer, *et al*., "SiGe Transformer Matched Power Amplifier for Operation at Millimeter-Wave Frequencies," *ESSCIRC*, Sept., 2005.

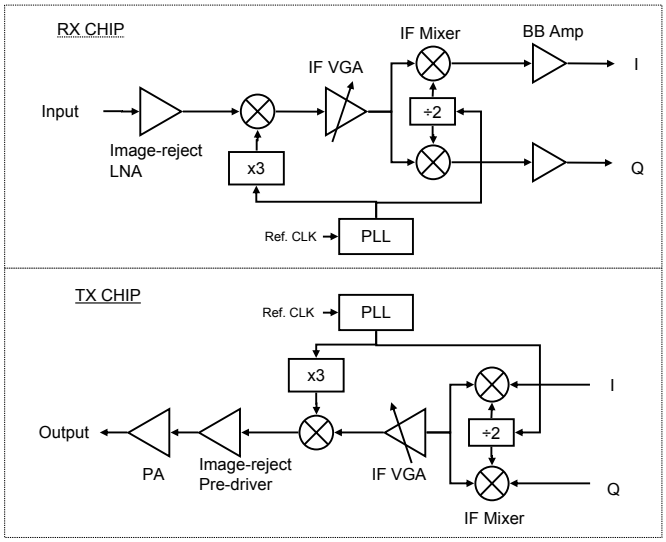

Figure 10.3.1: Block diagrams of the 60GHz RX and TX.

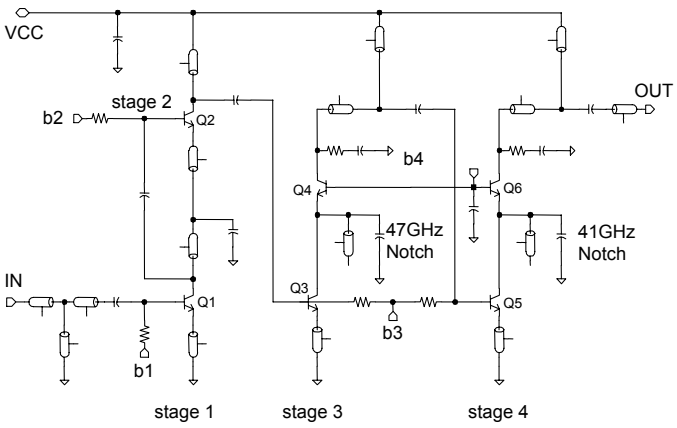

Figure 10.3.2: Schematic of the 60GHz image-reject LNA (bias details are not shown).

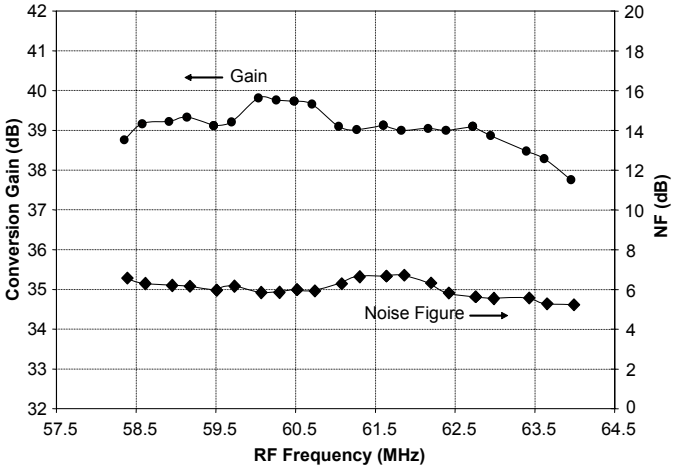

Figure 10.3.3: Measured NF and conversion gain of RX at 25˚C.

60-GHz Receiver Measurements		60-GHz Transmitter Measurements	
Gain	38-40 dB	Gain	34-37 dB
Noise Figure	5-6.7 dB	P_{1dB} (out)	10-12 dBm
S11, RF in	-15 dB	P_{sat}	16-17 dBm
Image Rejection	> 30 dB	Image Rejection	20-30 dB
P_{1dB} (in)	-36 dBm	PAE of PA	6-10%
IIP3	-30 dBm	Carrier Suppression	21-25 dB
3xLO leakage, RF in	< -77 dBm at 52-55 GHz	3xLO Spur	-25 to -20 dBm
Phase Noise (1MHz), tripled	-85 to -90 dBc/Hz < -130 dBc/Hz floor	Phase Noise, (1MHz) tripled	-85 to -90 dBc/Hz < -130 dBc/Hz floor
I/Q Balance	0-4 degrees <1dB	I/Q Balance	±2 deg ±0.5 dB
Power Dissipation	195 mA, 2.7 V	Power Dissipation	190 mA, 2.7 V 72 mA, 4.0 V

Figure 10.3.4: Measured performance summary for the RX and the TX across 59 to 64GHz ISM band at 25˚C.

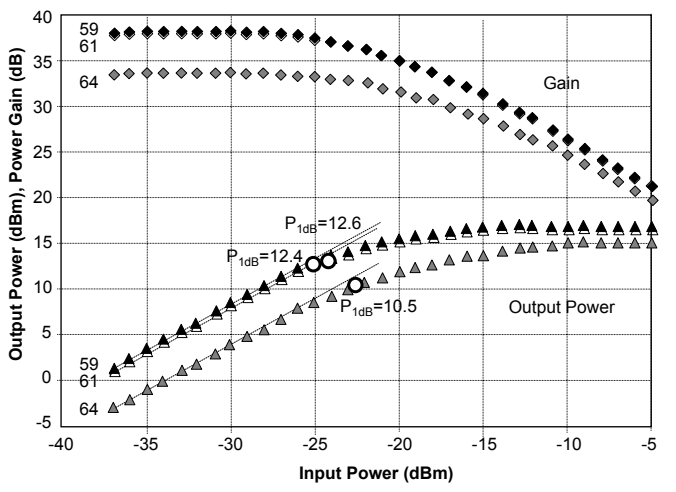

Figure 10.3.5: Measured output power and conversion gain of TX at 59, 61, and 64GHz, 25˚C.

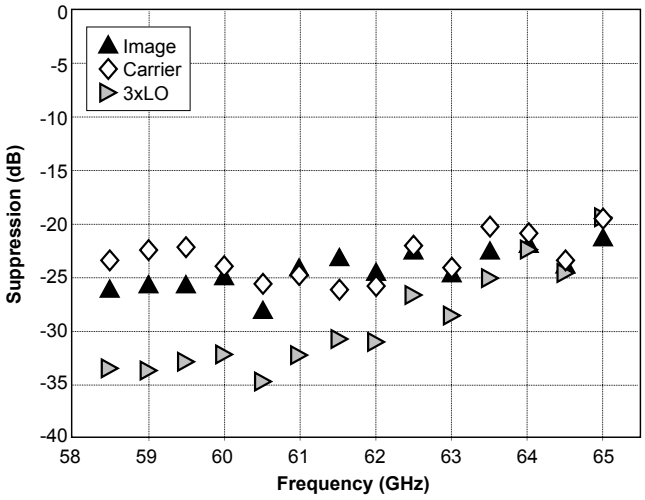

Figure 10.3.6: Measured spurious response of TX at -25dBm input power, 25˚C.

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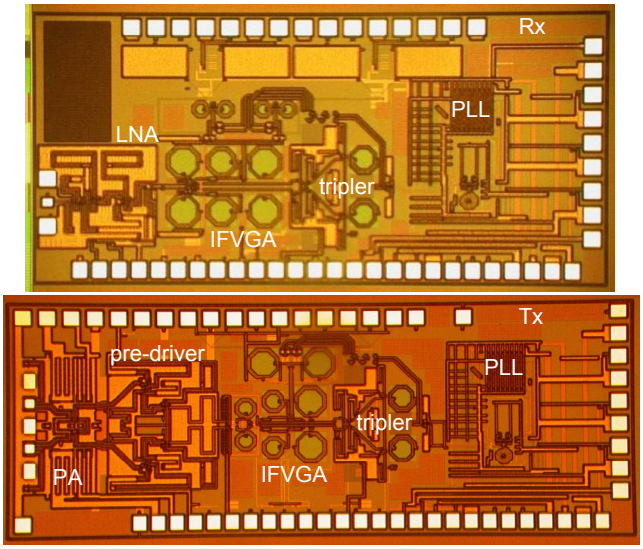

Figure 10.3.7: Die micrographs of the RX (top) and the TX (bottom).

